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An area efficient and low-power parallel processors on a chip

B. Sireesha[1], M. Jagadeesh[2] and Vijaya Sree[3]

[1]*Department of E. E. E., Annamacharya College of Engineering, India.*
[2]*Department of E. C. M., K. L. University, India.*
[3]*Department of E. C. E., C.V.R.C.E, India.*

Abstract

Multiprocessor system-on-chip (MPSoC) architectures have risen as a prevalent answer to the ever-increasing performance reduce the power consumption requirements, that are customized to a specific application have the potential to achieve efficient area, while additionally obliging low power consumption. The power consumed and area of the system majorly depends on the memory Communication medium of Processors, some issues involved in Memory communication of processors. In this Paper we avoid that issue and show two separate techniques to reduce the power consumption and area. The main technique is Scratch Pad Memory (SPM) replacement instead of cache replacement, second technique is Network on Chip (NOC) instead of Advanced Microcontroller Bus Architecture (AMBA) communication medium between processors.

Keywords: MPSOC, SPM, NOC, Hardware/Software co-design

1. Introduction

Now a day's embedded systems consist SRAM and DRAM. Maximum applications suitable to SRAM. In real time application caches are preferred in embedded systems, these cache architecture in embedded system more complex than general purpose processors. Embedded systems are characteristics application of SoC, micro controller and SoC both are same, micro controller contains RAM in a single chip system, SoC contains powerful processors which needs external memory. Many applications can't run single SoC with in time, then Multi-processor system on chip introduced, MPSoC can be used multi-application like communication, signal processing etc., each processor contains its own cache memory [1]. The architecture of MPSoC mainly contains three elements 1.Processing Elements, 2. Memory element and 3.communica-tion infrastructure, processing elements are two types one is Homogeneous when all PEs are same, another is heterogeneous when minimum one PE is different than others. MPSoC system tends to thousands of elements. As the size of MPSoC increase, we need to optimize the system several aspects like energy consumption and resource allocation, according to memory, we have three types of data memory 1.Cache Memory, 2.Scratch pad memory and 3.Main Memory.

First two memories are online memory, and main memory can be off-chip memory [2]. Present generation mainly using Cache memory, in that memory some issues involved like cache coherence. According to communication infrastructure so many busses transfer data one point to another point, when transferring data one place to another place some problem occurs.

In proposed paper to solve memory and communication issues using new replacement algorithm and efficient communication medium, the remaining of the paper some related work in section 2 and proposing technique, presented results in Section 3 and 4 followed by conclusion in section 5.

2. Literature Survey

Soutav Roy presented a new cache replacement policy called Hierarchical Non-Most-Recently-Used (H-NMRU). For most of the embedded processors H-NMRU provides low area and high performance cache replacement policy. This cache replacement policy saves substantial area and provides similar performance to LRU and PLRU [3]. The most attractive option among the available policies is H-NMRU. As the initial state of the cache, when program execution may impact the number of cache hits and misses [4]. Jan Reineke and Daniel

Corresponding author: B. Sireesha
Email Id: naresh.klu@gmal.com

Grand have designed a device which can precisely calculate sensitivity measurements of replacement policies such as LRU, FIFO, PLRU and MRU. The initial state of FIFO, PLRU or MRU will have a large impact on the cache performance [5]. This model of execution time is used to evaluate the impact of cache sensitivity on measured execution times. Huaxi Gu1 proposed a 5X5 cost router which consumes less power, low loss and cost efficient device called Cygnus or optical NoC. Cygnus is non-blocking and based on silicon micro resonators [6]. In multiprocessor system-on-chip (MPSoC) NoC can improve the bandwidth and power efficiency. However, traditional metallic interconnects consume a significant amount of power to deliver even higher communication bandwidth required in the near future. Huaxi Gu recommended a fat tree-based optical NoC (FONoC) with its topology, floorplan, con-ventions, and an ease optical switch which occupies less power, optical turn around switch (OTAR) [7]. Unlike other optical NoC, FONoC does not need to build a different electronic NoC for system control. The Evolution of SOC Interconnect and How NOC Fits within It, SoC is on chip connection, there are more complex, these SoC interconnecting medium which one is best explained Bruce Mathewson [8].

3. Proposed Policy

Cache performance and communication medium both are important role in multi-processor system on chip, based on these two issues we propose two policies, one is cache re-placement policy another efficient communication among on chip systems.

3.1 Replacement Policy

In present days, data storing at a cache in multi-processor system on chip, when cache memory was full at that time one wants access extra data from shared memory or external disk, we are using some replacement algorithm like Random, Fist in First Out (FIFO), Least Recently Used (LRU). Re-placement strategy characterized as the algorithm or approach to choose target memory block desires to be replaced and save in memory when memory block need to be allotted. If use Random method, randomly choose one old block from the cache memory and swapped with new block, this method occurs high cache miss rate happens, In FIFO method replace old block from the cache memory and swapped with new blocks, this method reduce cache miss rate than random, in LRU substitution strategy deals with the idea of FIFO method, least recently used block from the cache memory and swapped with new blocks, on account of a cache miss, the retrieved data portion is located in the front of the queue and the last data portion from the queue is detached as the least recently used data portion present in the queue. While on the account of cache hit, the data portion which has previously existed anyplace in the queue is swapped to the front in the queue [9]. When it happens entire processor performance reduces. Replacement policy is an alternative critical issue which influences the speed and execution of memory. Therefore, finding the best replacement policy for cache memory in multi-processor system on chip, that is cache and SPM is the fundamental interest. For that reason, the aim is to search suitable solutions for cache and on chip SPM memory problems.

To solve the issues of on-chip scratch pad memory, three replacement policies and cache memory presented. Size of SPM is considered as very little when associated to cache memory. Here, processor first checks the accessibility of data in SPM and data is not available in SPM, it strives for cache memory. This Proposal will implement replacement policies in SPM for the first time.

3.2 Communication issues in Multi-processor System on chip

In multi-processor system on chip contains number of homogeneous or heterogeneous processors, these processors exchanging data or access data from shared memory need communication interface as AMBA, it good communication and each component has its own particular capacity. It has some drawbacks like crossbar communication, permits just homogeneous processors [10]. Then to solve these problems we propose Network on chip, it is a communication subsystem on an incorporated circuit between IP cores in a system on chip. NoC innovation applies organizing hypothesis and strategies to on-chip correspondence and brings striking upgrades over routine transport and crossbar interconnections. NoC enhances the versatility of SoC, and the force proficiency of complex SoC contrasted with different outlines.

4. Experimental Setup and Evaluation

The performance of a multi-processor system on chip calculated by the simple scalar simulator, it affords an infrastructure for simulation and architectural modeling. We planned the SPM through a statically declared array. Performance assessment of different cache replacement policies Random, FIFO and LRU has been carried out utilizing simulators from the alpha form of the tool-set and later stretched out to execute proposed substitution arrangement. In this work, we have analyzed two models, one with a store also, second with a scratchpad memory and additionally store. Simulator simulates replacement policies Random, FIFO and LRU of cache memory and scratch pad memory, simulation has been performed for Cache and SPM organized 1,2,4,16 way associativity in conjunction with an altered mixture of replacement policies. Table 1. Consists of the Cache miss rate values for matrix multiplication benchmark. To determine and estimate the best replacement policy, we show a graph for associativity values 1 and 16 for both SPM and cache from the considered values in Fig 1. Finally, we agreed from the graph LRU is the lowest miss rate among three replacement algorithms.

Table 1: Miss rate SPM & cache

	SPM			Cache emory		
	Random	FIFO	LRU	Random	FIFO	LRU
1	0.437	0.436	0.435	0.71	0.69	0.68
2	0.35	0.345	0.34	0.6	0.58	0.54
4	0.24	0.22	0.22	0.45	0.42	0.4
6	0.12	0.115	0.112	0.25	0.22	0.18

While using SPM the efficiency miss rate is up to 62%. The table 2 shows the efficiency values of all the three replacement policies and the average of miss rate. As per the results obtained it is clear that there is clear increase and decrease in associativity of cache miss rates. Furthermore, outcome of using scratch pad memory becomes stronger in a system of high value of memory associativity

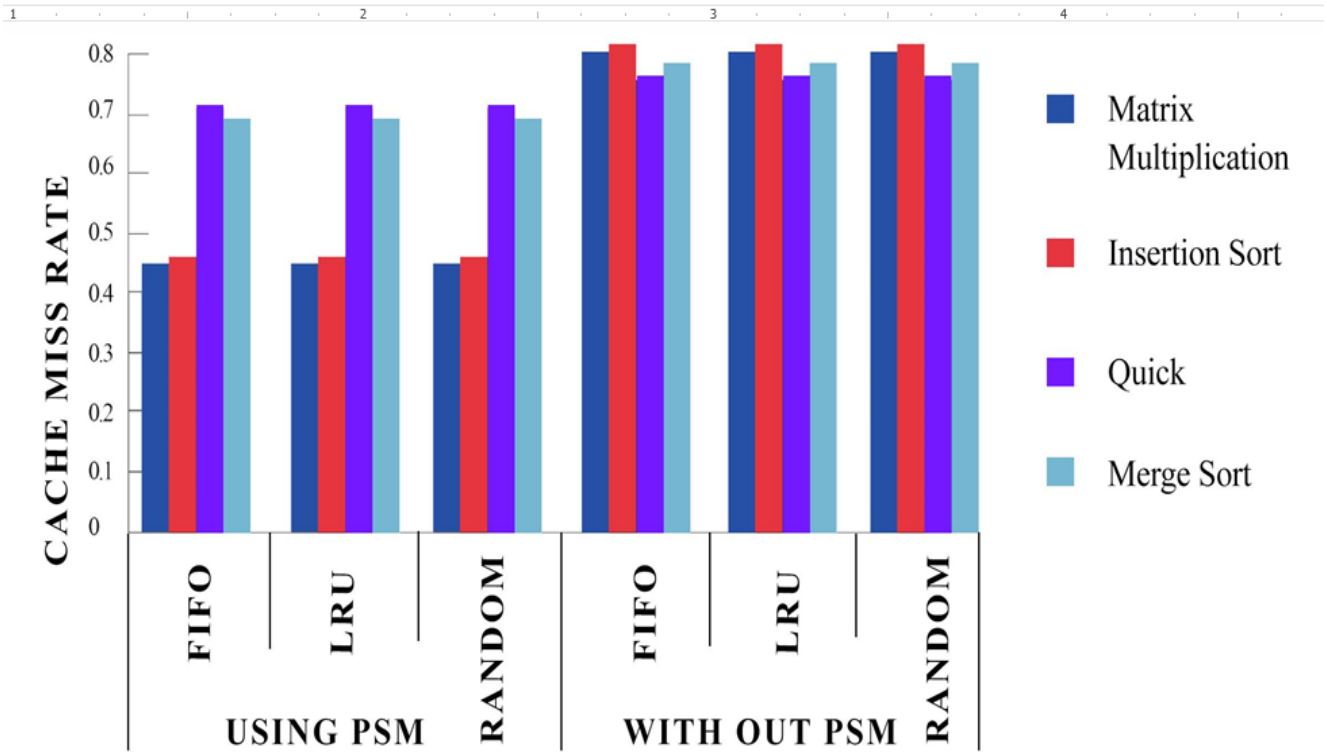

Figure 1: Replacement Technique

To solve previous communication problem, Network on chip as a communication interface between multi-processor systems on chip presented. By using Network on Chip (NoC) links, we can reduce the complexity of designing and it provides predictable speed, power, noise, reliability, etc. A net-work is a natural architectural choice from the system design view point with the advent of multi-core processor systems. A NoC can provide support for modularity and IP reuse via standard interfaces, and handles synchronization issues. Finally NOC serve as a platform for system test, hence, increase engineering productivity. When we compared to previous communication interface AMBA, it is good communication and each component has its own particular capacity. It has some drawbacks like crossbar communication, permits just homogeneous processors, but Network on chip is point to point communication and allows homogeneous and heterogeneous processors. Particularly when we compared area, performance between AMBA and NOC, by using Synopses Design Compiler we have obtained the implementation results (area, power consumption, performance), and also performed place and route using Synopsis IC compiler. The implementation evaluation results are illustrated in Fig 2.

Table 2 : Performance

Standard	Associativity	Avg Miss Rate using SPM	Avg Miss Rate using Cache	% Avg Miss Rate Improvement
Mat Mult.	1	0.435	0.682	20.15%
Insertion sort		0.454	0.691	
Quick		0.482	0.724	
Merge Sort		0.495	0.741	
Mat Mult.	2	0.34	0.54	36.65%
Insertion sort		0.353	0.568	
Quick		0.382	0.592	
Merge Sort		0.397	0.62	
Mat Mult.	4	0.22	0.4	54.12%
Insertion sort		0.243	0.423	
Quick		0.251	0.432	
Merge Sort		0.263	0.465	
Mat Mult.	16	0.112	0.18	62.34%
Insertion sort		0.125	0.196	
Quick		0.12	0.19	
Merge Sort		0.103	0.16	

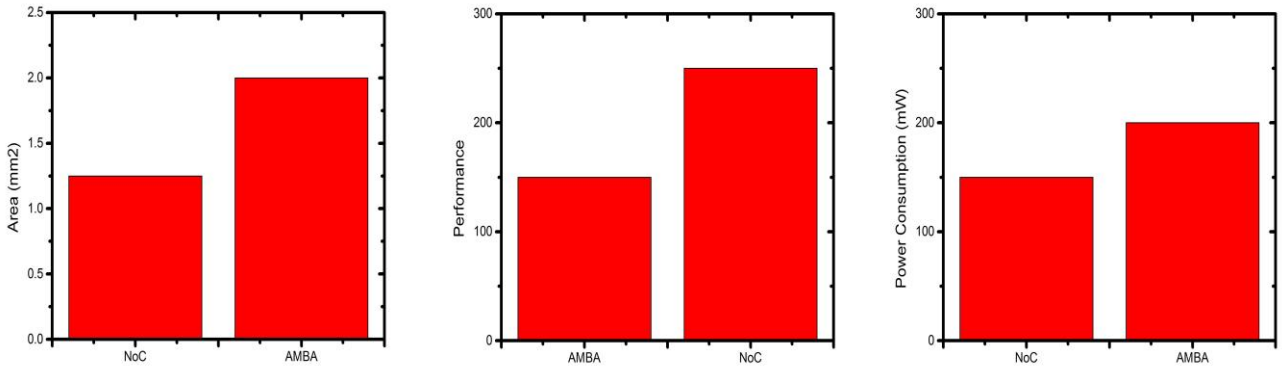

Figure 2: Implementation results

5. Conclusion

In this paper we avoid that issue and show two separate techniques to increase performance reduce the Power consumption. The first technique is Scratch Pad Memory (SPM) Replacement rather than cache replacement, here we represented evaluation of cache with scratch pad memory using simulations by improving designs of main memory issues like MPSOC association and its replacement policies. Due to use of SRAM there is a reduction of up to 62% in cache miss rate in our simulation results that are demonstrated. Hence, system will be more efficient and will have less no of miss rates due to addition of on-chip memory SPM. Second technique is Network on Chip (NOC) rather than Advanced Microcontroller Bus Architecture (AMBA) communication medium between processors. Got good performance, area and efficient power consumption

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